

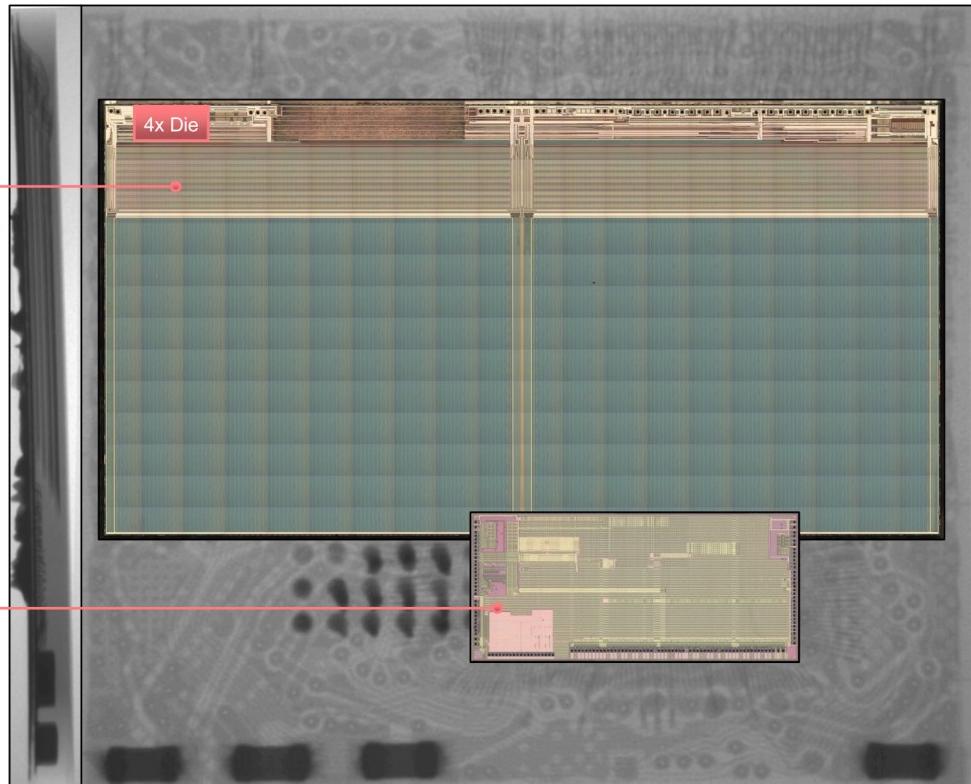
EXHIBIT F

U.S. Patent No. 6,724,241 (“241 Patent”)**Accused Products**

LG products with SanDisk/Toshiba 64L 3D NAND flash chips, including without limitation the LG V50 ThinQ (“Accused Products”), infringe at least Claims 1-3, 6-8, and 11 of the ’241 Patent.

Claim 1

Claim 1	Accused Product
[1pre] 1. A charge pump circuit for generating a charge pump voltage having minimal voltage ripples, comprising:	<p>To the extent the preamble is limiting, each Accused Product includes a charge pump circuit for generating a charge pump voltage having minimal voltage ripples.</p> <p>For example, the V50 ThinQ includes the charge pump circuit of the SanDisk/Toshiba 3D NAND flash chip, die identifier FRN1256G.</p> <p><i>See, e.g.:</i></p>

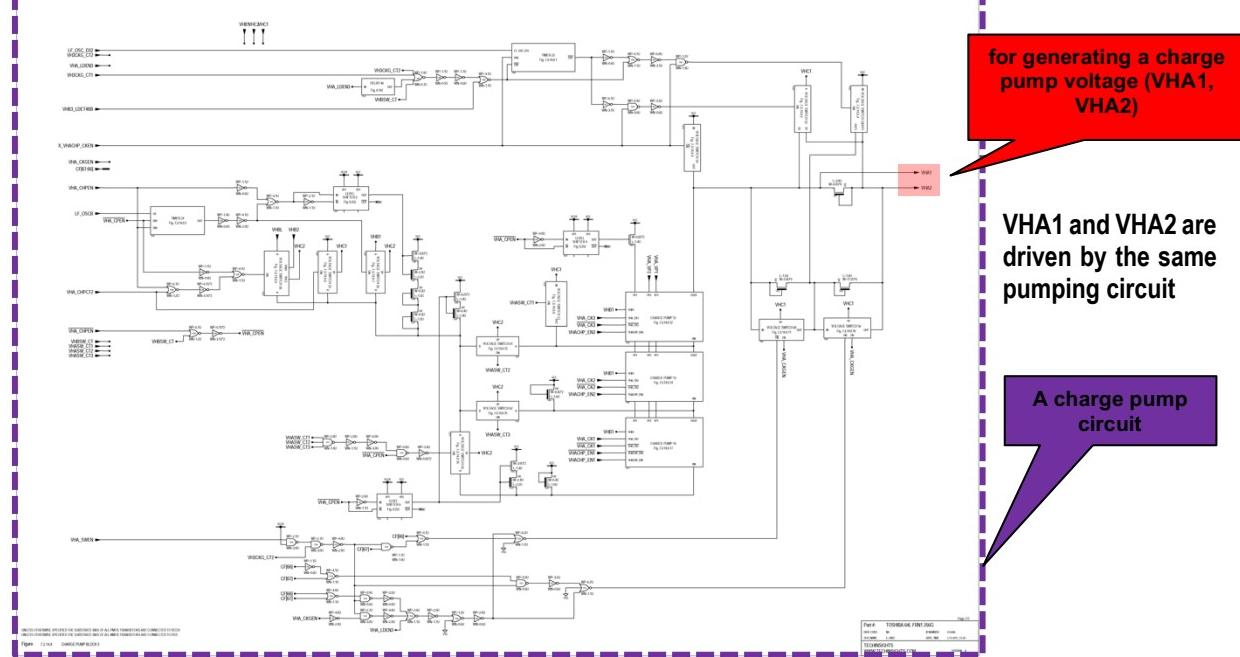
Claim 1	Accused Product
	 <p>3 - SanDisk #SDINDDH4-128G Multichip Memory - 128 GB 3D TLC NAND Flash, Memory Controller (UFS 2.1) (5-Die Pkg.) Pkg Size: 13 x 11.51 mm</p> <p>3.1 - SanDisk #FRN1256G 3D TLC NAND Flash Memory - 32 GB Die Size: 12.16 x 6.26 mm</p> <p>3.2 - SanDisk #EAGLEMP28 Memory Controller (UFS 2.1) Die Size: 5.02 x 2.27 mm</p> <p>Function: Memory: Non-Volatile</p> <p>Source: TechInsights Deep Dive Teardown, LG V50 ThinQ 5G LM-V450VMB ID355205-DLf</p>

Claim 1

Accused Product

**VHA1
VHA2**

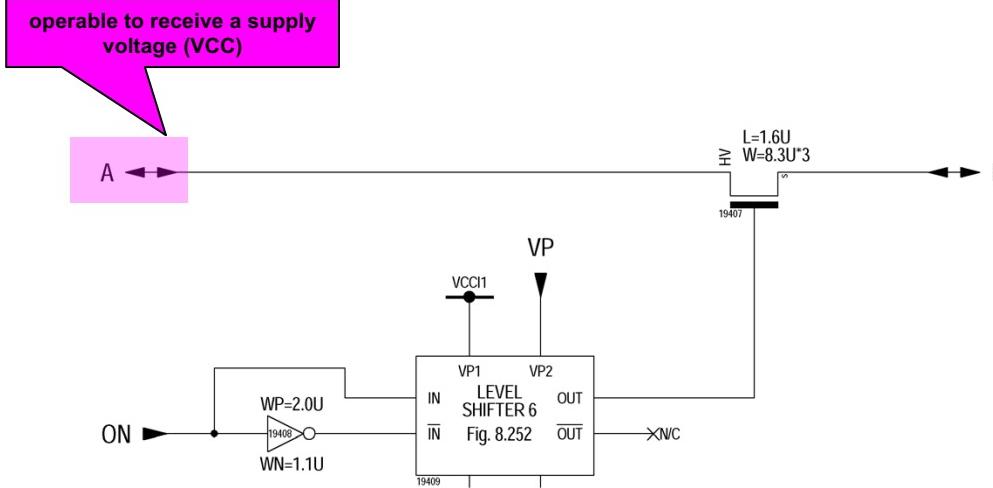
A charge pump circuit

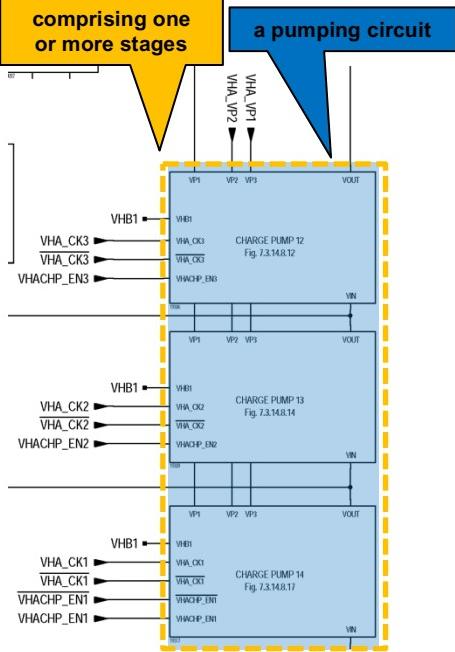
Claim 1	Accused Product
	 <p data-bbox="635 997 1839 1070">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5</p>

Claim 1	Accused Product
	<p style="color: red; font-weight: bold;">Charge pump output voltage VHA2 is provided to high voltage switches to selectively drive PNWELL.</p>

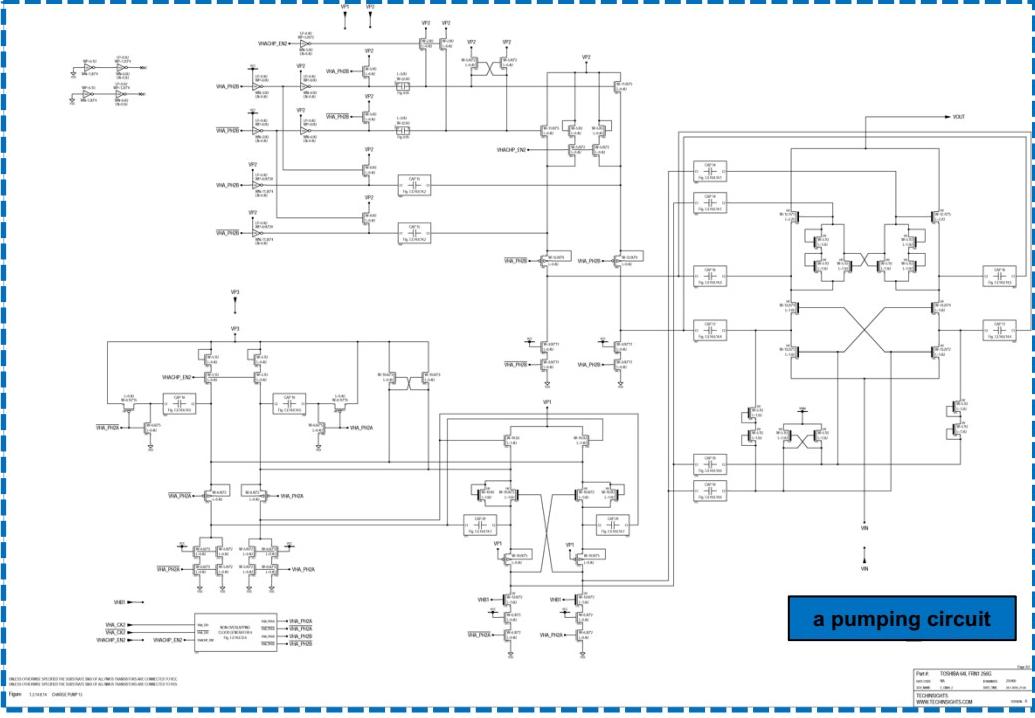
Claim 1	Accused Product
	<p>Charge pump output voltage VHA1 is provided to high voltage switches to selectively drive wordline circuits.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
1[a] a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages;	<p>Each Accused Product includes a pumping circuit comprising one or more stages operable to receive a supply voltage and generate a selected one of a plurality of pump voltages.</p> <p>For example, in the pumping circuit, 1, 2, or 3 main stages can be enabled for operation. Supply voltage can be selected from external VCC or internally generated pumped voltages VHBL or VHBL. VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out</p>

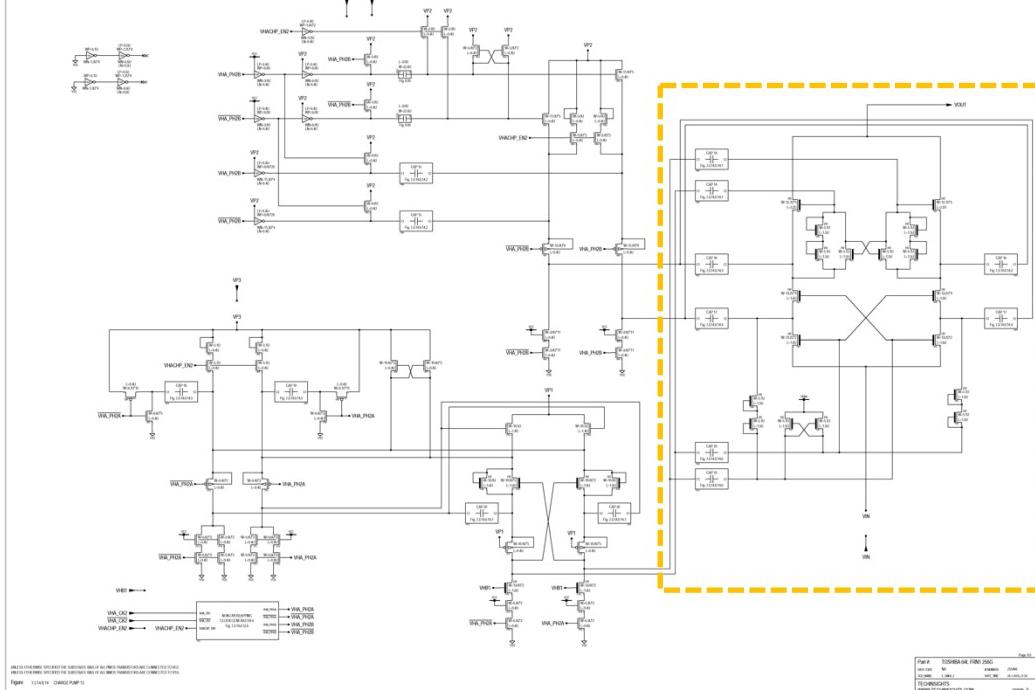
Claim 1	Accused Product
	<p>resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. VHA_CK2 and VHA_CK2* drive the middle stage of the pumping circuit. VHA_PH2 non-overlapping clocks drive Charge Pump 13. When VHA_PH2 clocks are suspended the pump stops operating so that VHA1 is limited to the voltage set by the level detector.</p> <p><i>See, e.g.:</i></p>

Claim 1	Accused Product
	<p>operable to receive a supply voltage (VCC)</p>  <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.6 Voltage Switch 55</p>

Claim 1	Accused Product
	 <p>comprising one or more stages</p> <p>a pumping circuit</p> <p>VHB1 VHA_CK3 VHA_CK3 VHACHP_EN3</p> <p>VHB1 VHA_CK2 VHA_CK2 VHACHP_EN2</p> <p>VHB1 VHA_CK1 VHA_CK1 VHACHP_EN1</p> <p>CHARGE PUMP 12 Fig. 7.3.14.8.12</p> <p>CHARGE PUMP 13 Fig. 7.3.14.8.14</p> <p>CHARGE PUMP 14 Fig. 7.3.14.8.17</p> <p>VIN</p> <p>VOUT</p> <p>VIN</p> <p>VOUT</p> <p>VIN</p> <p>VOUT</p> <p>VIN</p> <p>VIN</p>

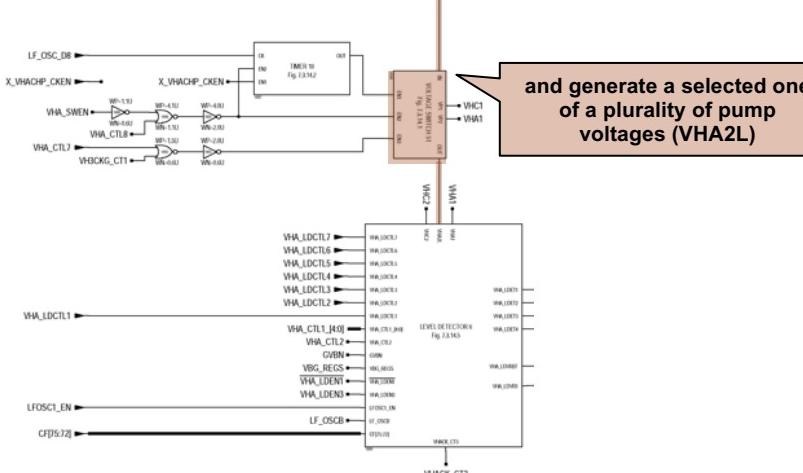
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block 5

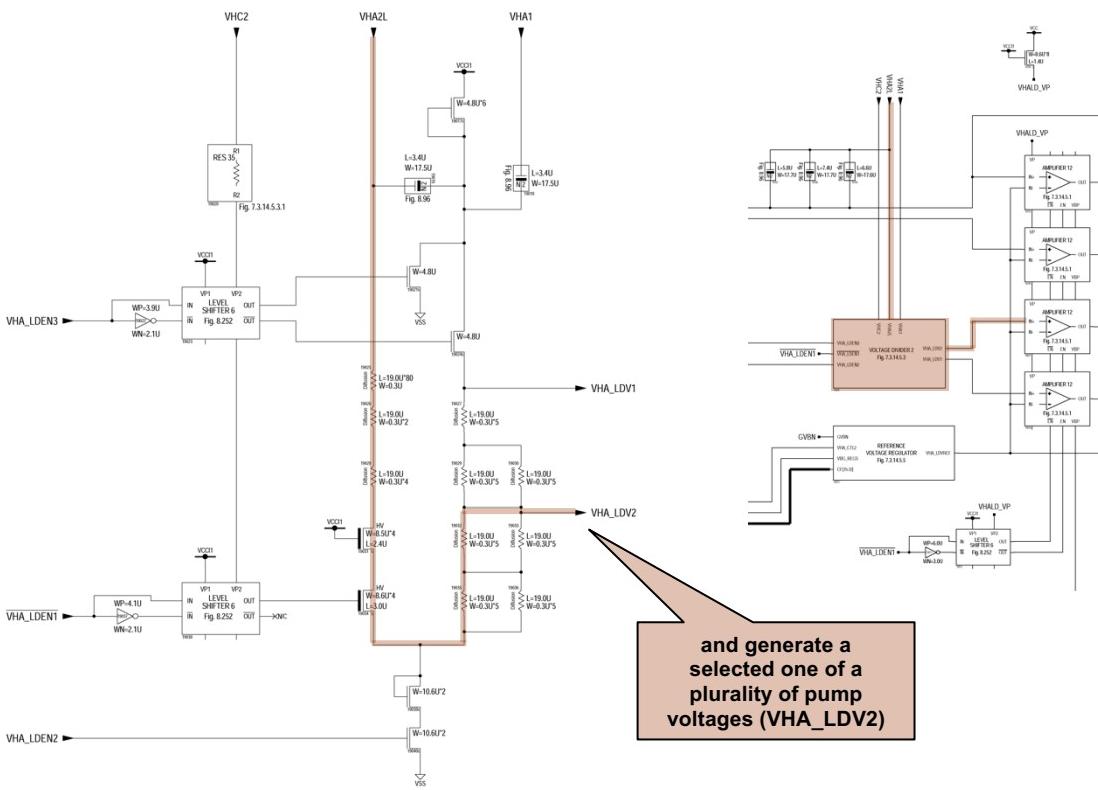
Claim 1	Accused Product
	 <p data-bbox="1453 882 1643 907">a pumping circuit</p> <p data-bbox="1558 948 1685 992">Part: TOSHIBA 05138_064G Date: 2020-06-10 TechInsights: www.techinsights.com</p> <p data-bbox="650 1041 1839 1114">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

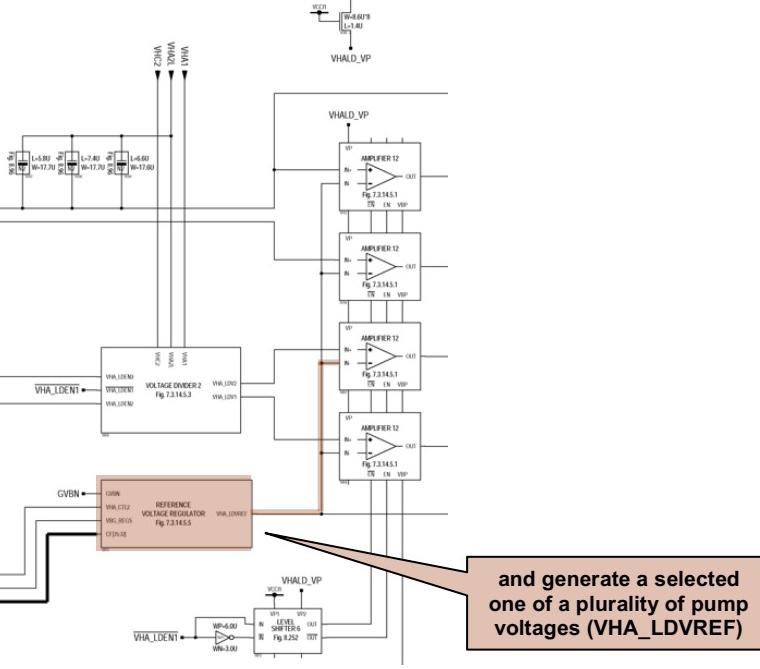
Claim 1	Accused Product
	 <p data-bbox="635 964 1670 980">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

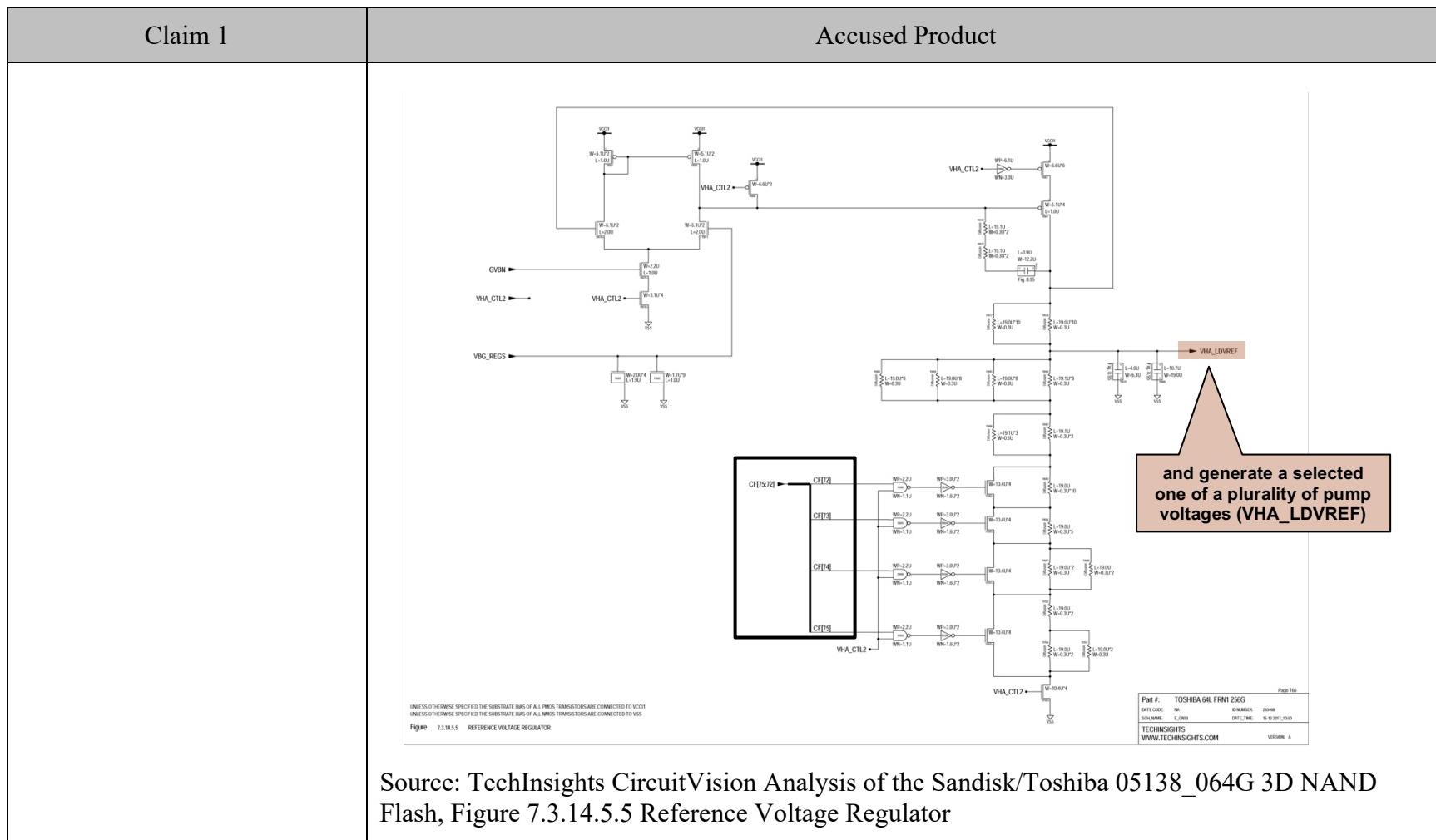
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

Claim 1	Accused Product
	<p>The diagram illustrates a voltage switch circuit (VHA2) and its control logic. The main circuit consists of a series of inductor and diode pairs connected to a central node. A red box highlights a section of the circuit with the label: and generate a selected one of a plurality of pump voltages (VHA2L). The control logic at the bottom includes three enable inputs (EN1, EN2, EN3), three switches (WP-1.5U, WP-2.0U, WP-2.1U), and a driver (DRIVER 24 OUT). The driver outputs VP1 and VP2, which are connected to the central node via inductors L=0.3U and L=19.1U.</p>

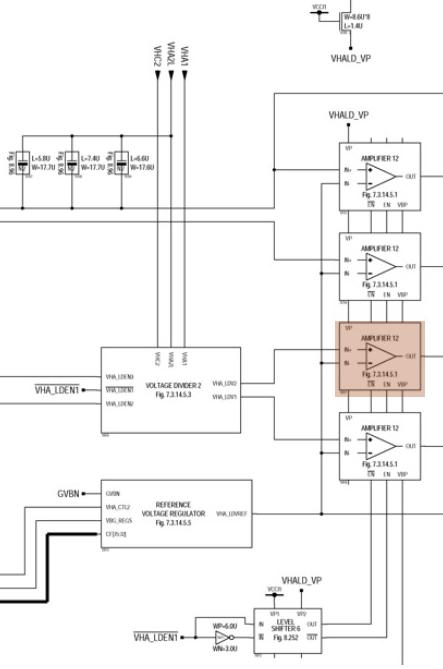
Claim 1	Accused Product
	 <p data-bbox="1161 391 1478 456">and generate a selected one of a plurality of pump voltages (VHA2L)</p> <p data-bbox="633 832 1837 897">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

Claim 1	Accused Product
	 <p data-bbox="650 1109 1848 1183"> Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6 </p>

Claim 1	Accused Product
	 <p>The diagram illustrates a circuit for generating selected pump voltages. It starts with a REFERENCE VOLTAGE REGULATOR (VRA_00000) receiving VGBN and VRA_CU2. Its output VRA_REF05 is connected to the non-inverting input (V+) of four AMPLIFIER 12 (Fig. 7.3145.1). The inverting inputs (V-) of these amplifiers receive signals from a VOLTAGE DIVIDER 2 (VRA_00001). The VOLTAGE DIVIDER 2 has four parallel branches with resistors labeled $R_{L=5.00}$, $R_{L=7.00}$, $R_{L=7.40}$, and $R_{L=6.00}$. The outputs of these branches are labeled VRA_10MA, VRA_12MA, VRA_17MA, and VRA_18MA. The outputs of the amplifiers are labeled VHALD_VP. A logic block at the bottom, labeled VHALD_VP (Fig. 8.252), takes the outputs of the amplifiers and the VRA_REF05 signal to generate a selected pump voltage VHA_LDVREF.</p> <p>and generate a selected one of a plurality of pump voltages (VHA_LDVREF)</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.5 Reference Voltage Regulator

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

Claim 1

Accused Product

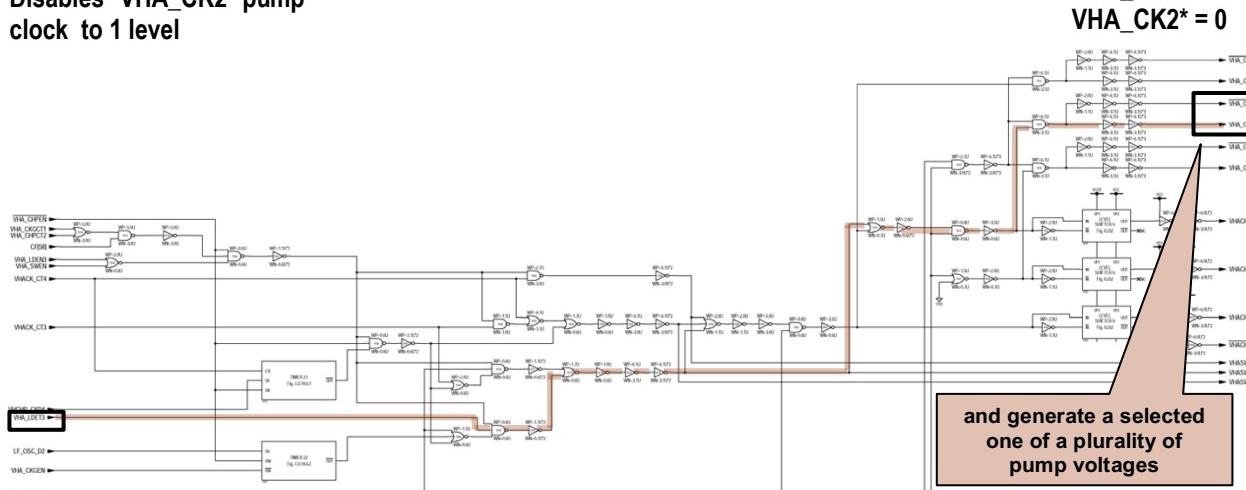
and generate a selected one of a plurality of pump voltages

VHA_LDET3 = 0

UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL PNP TRANSISTORS ARE CONNECTED TO VSS
UNLESS OTHERWISE SPECIFIED THE SUBSTRATE BIAS OF ALL NMOS TRANSISTORS ARE CONNECTED TO VDD

Figure 7.3.145 LEVEL DETECTORS

Part #: TOSHIBA 04LFRN1254G
REV CODE: NA
SERIAL #: 20000
DATE CODE: 26.09.2016
TECHNOLOGY: 0.13µm
WEBSITE: WWW.TECHINSIGHTS.COM

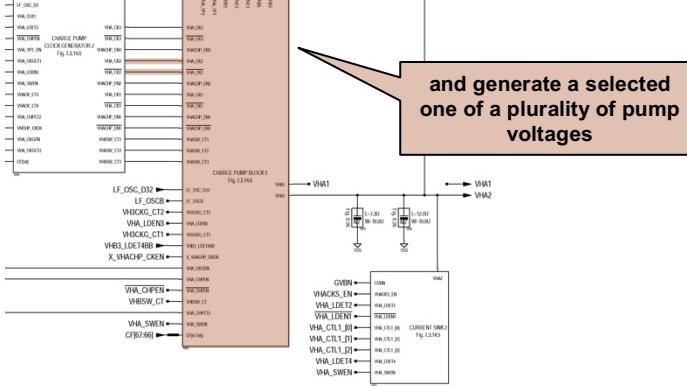
Claim 1	Accused Product
	<p>VHA_LDET3 = 1 Disables VHA_CK2 pump clock to 1 level</p>  <p>VHA_CK2 = 1 VHA_CK2* = 0</p> <p>and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.6 Charge Pump Clock Generator 2</p>

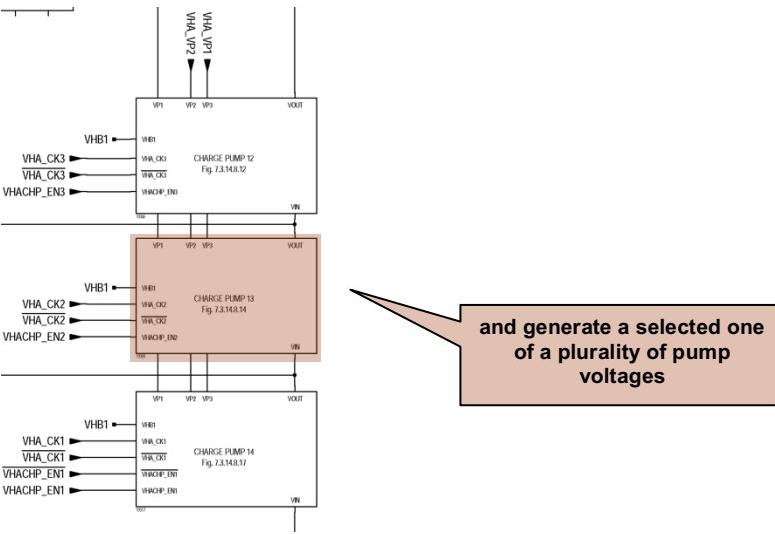
Claim 1

Accused Product

and generate a selected one of a plurality of pump voltages

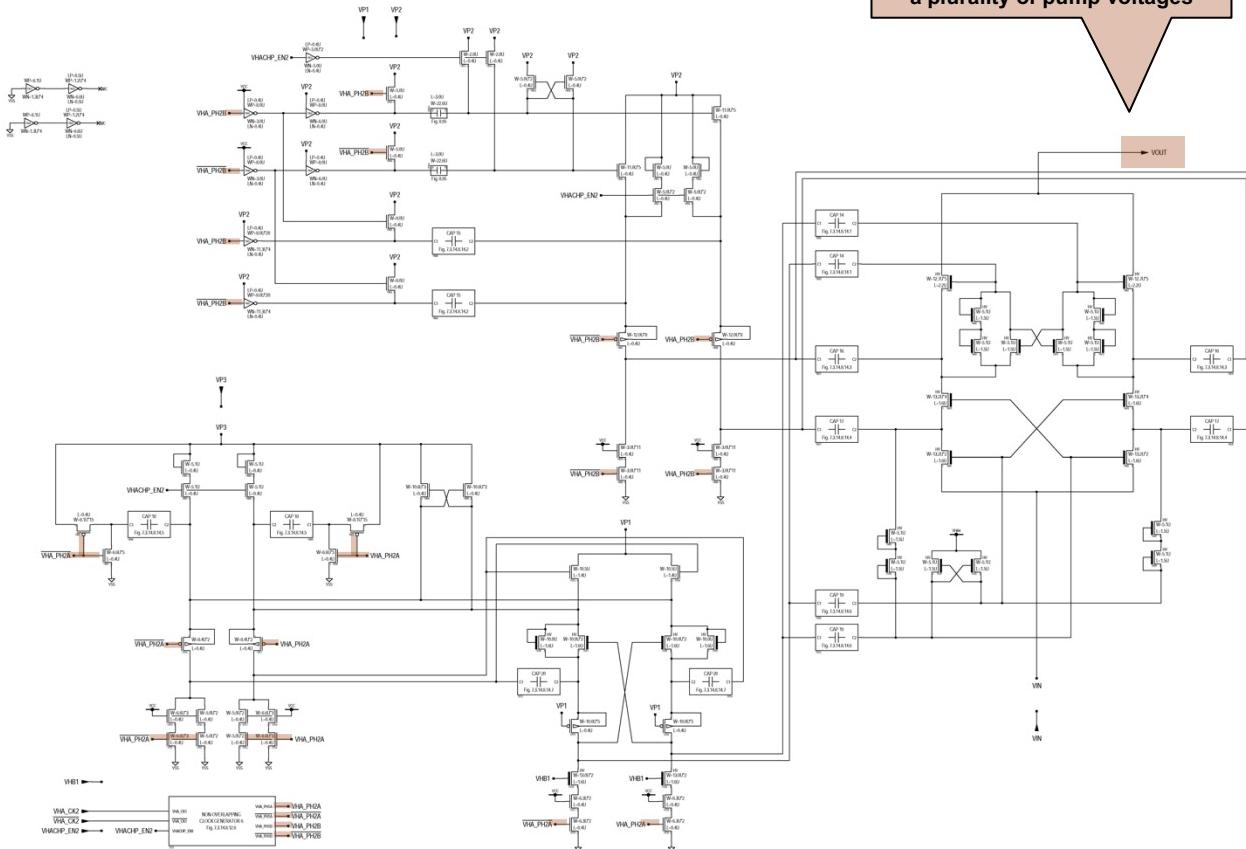
Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4

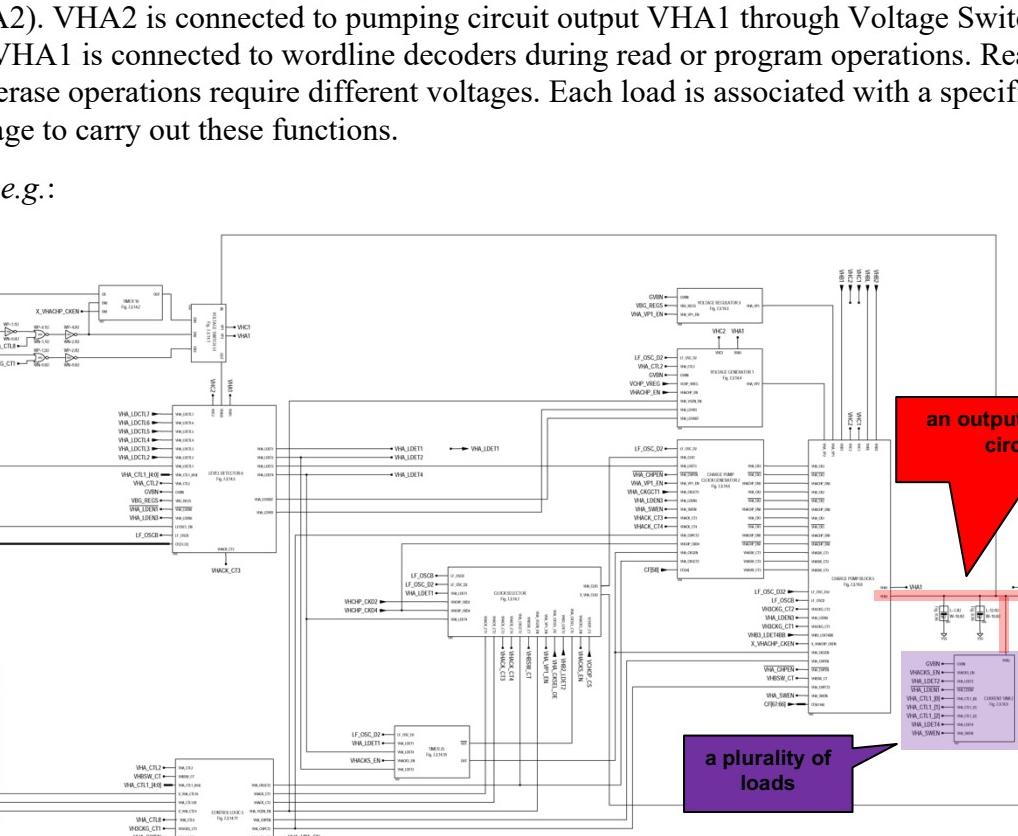
Claim 1	Accused Product
	 <p data-bbox="1151 220 1383 244">and generate a selected one of a plurality of pump voltages</p> <p data-bbox="633 701 1837 775">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14 Charge Pump Block 4</p>

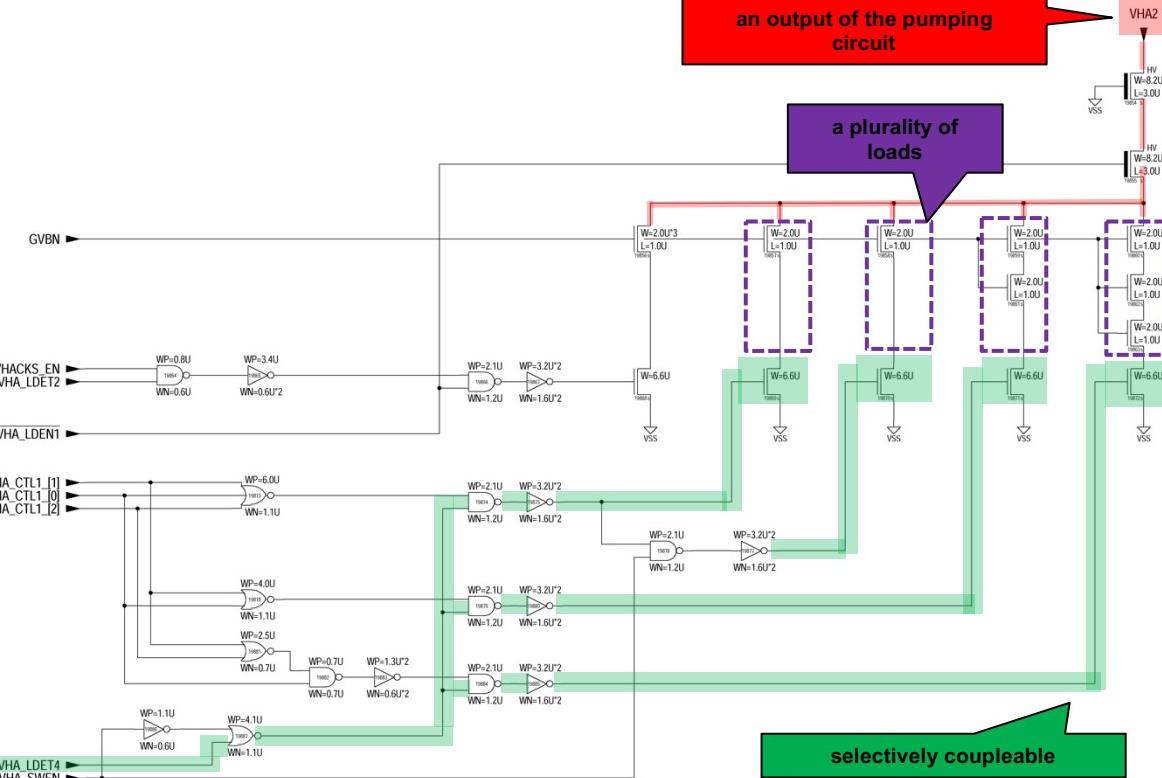
Claim 1	Accused Product
	 <p>The diagram illustrates three vertically stacked Charge Pump blocks, labeled 12, 13, and 14, each with its own set of pins and control signals. Each block has three output pins (V1, V2, V3) and one output pin (VOUT). The top block (12) is labeled "CHARGE PUMP 12 Fig. 7.3.14.32". The middle block (13) is labeled "CHARGE PUMP 13 Fig. 7.3.14.34". The bottom block (14) is labeled "CHARGE PUMP 14 Fig. 7.3.14.17". Control signals include VHB1, VHA_CK1, VHA_CK2, VHA_CK3, VHACHP_EN1, VHACHP_EN2, and VHACHP_EN3. A callout box points to the bottom block (14) with the text: "and generate a selected one of a plurality of pump voltages".</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8 Charge Pump Block</p>

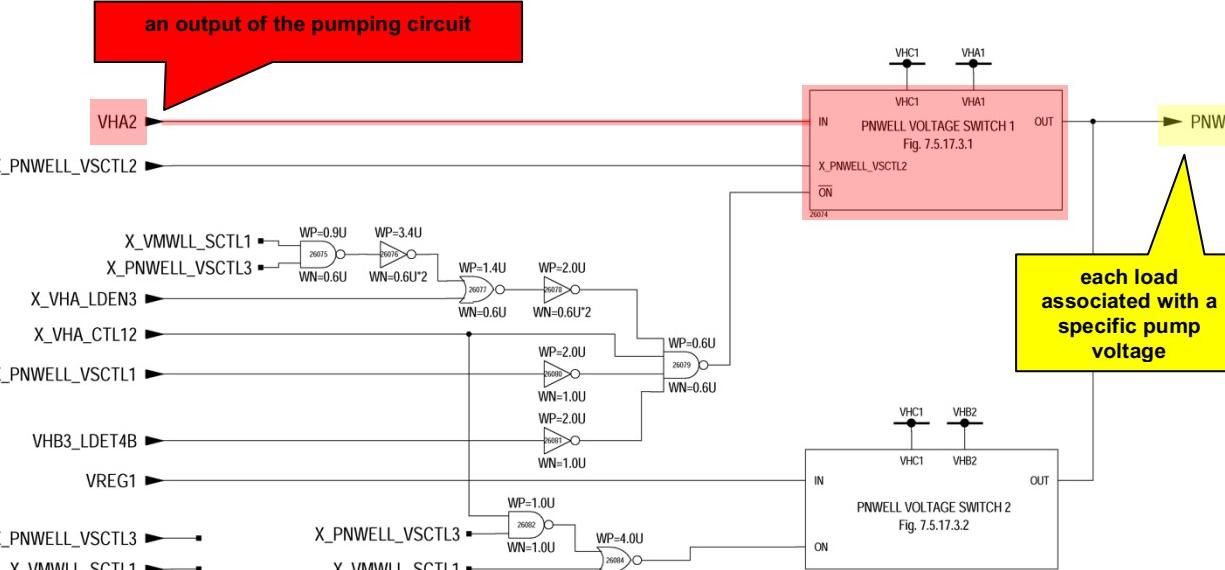
Claim 1	Accused Product
	<p>VHA_CK2 VHA_CK2*</p> <p style="text-align: right;">VHA_PH2A VHA_PH2A* VHA_PH2B VHA_PH2B*</p> <p style="text-align: right;">and generate a selected one of a plurality of pump voltages</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.12.6 Non-Overlapping Clock Generator 6</p>

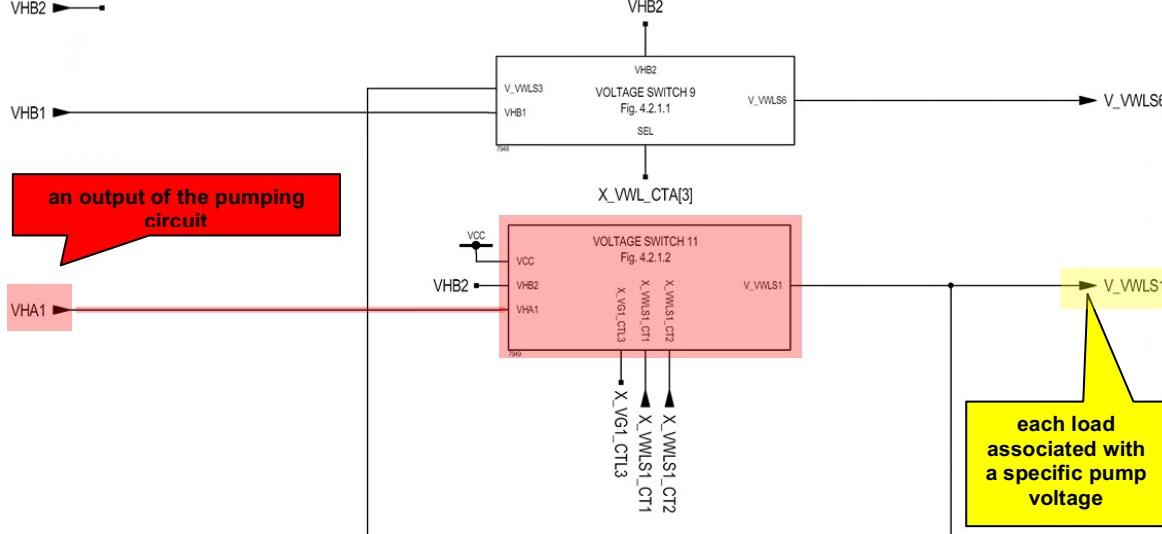
Claim 1	Accused Product
	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>

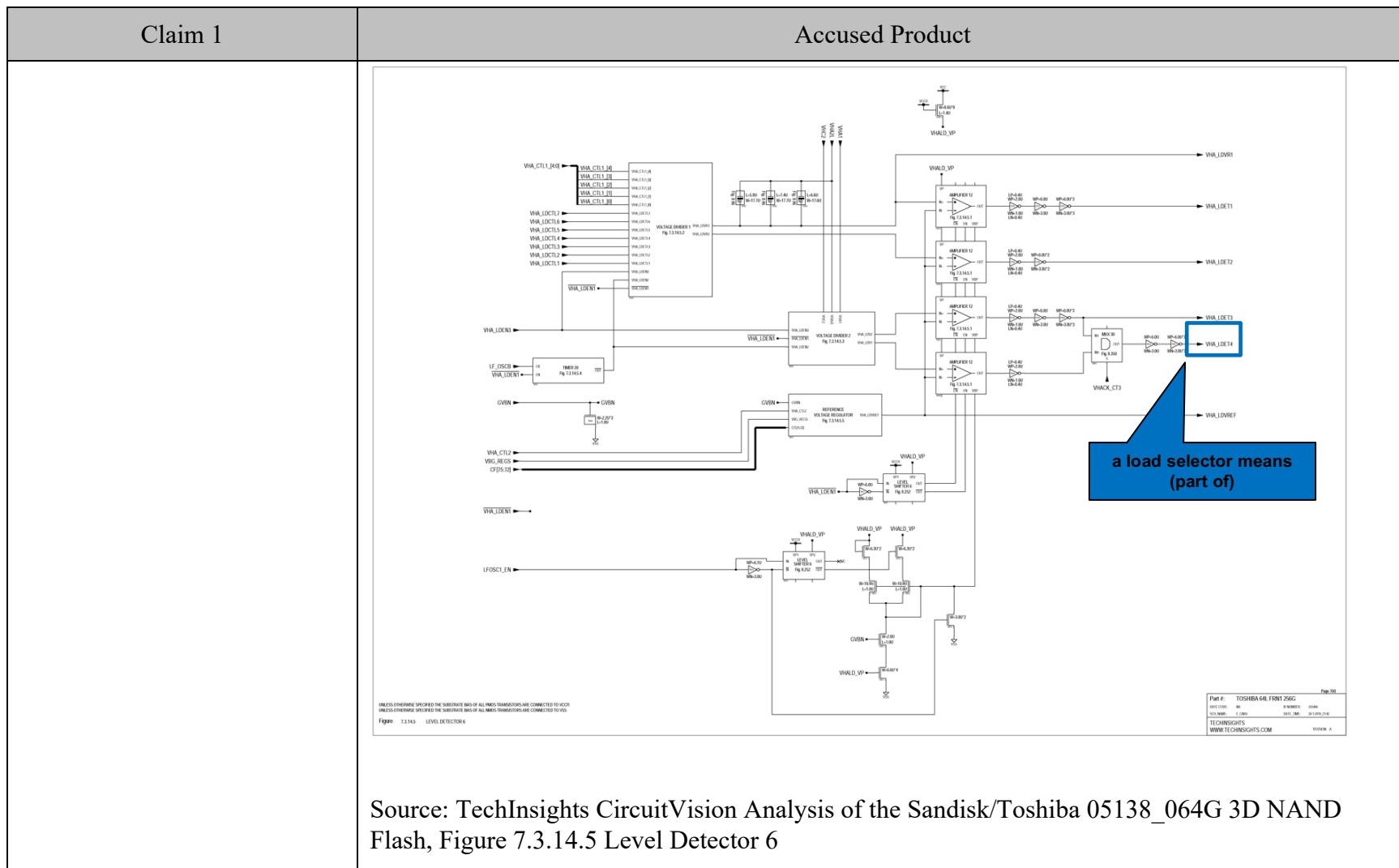
Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.8.14 Charge Pump 13</p>
1[b] a plurality of loads selectively coupleable to an output of the pumping circuit,	Each Accused Product includes a plurality of loads selectively coupleable to an output of the pumping circuit, each load associated with a specific pump voltage.

Claim 1	Accused Product
<p>each load associated with a specific pump voltage; and</p>	<p>For example, VHA2 is an output of the pumping circuit. A plurality of loads (contained within Current Sink 2) can be selectively coupled to an output of the pumping circuit (for example VHA2). VHA2 is connected to pumping circuit output VHA1 through Voltage Switches 59 and 60. VHA1 is connected to wordline decoders during read or program operations. Read, program and erase operations require different voltages. Each load is associated with a specific pump voltage to carry out these functions.</p> <p><i>See, e.g.:</i></p>  <p>The diagram illustrates the internal structure of the Charge Pump Block 4. It features several pumping circuits, each consisting of an oscillator (LF_OSC_1, LF_OSC_2, LF_OSC_3, LF_OSC_4) and a voltage generator (VGA_VREF, VGA_VPT_EN). These generate various pump voltages (VHA1, VHA2, VHA3, etc.) which are then distributed to a variety of loads. The loads include wordline decoders (WLD), charge pumps (CP), and current sinks (CS). A red speech bubble points to the output VHA2, labeled as 'an output of the pumping circuit'. A purple speech bubble points to a cluster of nodes labeled 'a plurality of loads'.</p>

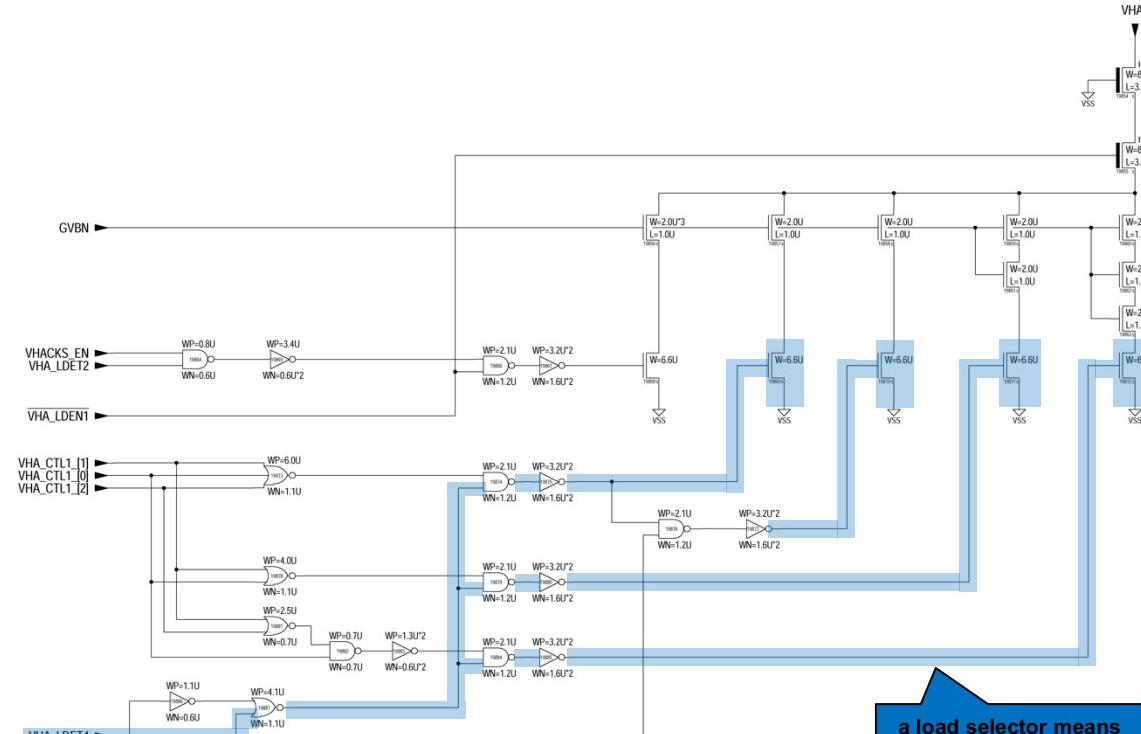
Claim 1	Accused Product
	 <p>The diagram illustrates a pumping circuit architecture. On the left, input signals include GVBN, VHACKS_EN, VHA_LDET2, VHA_LDEN1, VHA_CTL1[1], VHA_CTL1[0], VHA_CTL1[2], and VHA_LDET4/VHA_SWEN. These signals pass through various logic stages (involving AND gates, OR gates, and inverters) before reaching a central pumping unit. The pumping unit consists of four parallel paths, each featuring a current source (labeled W=6.6U) connected to ground (VSS). The outputs of these paths are labeled W=2.0U L=1.0U. A red callout box points to one of these outputs with the text "an output of the pumping circuit". A purple callout box points to the four parallel paths with the text "a plurality of loads". A green callout box at the bottom right points to the pumping unit with the text "selectively coupleable". The circuit is designed to manage multiple loads (VHA2, VHA1, VHA0, VHA3) via control signals and selective coupling.</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

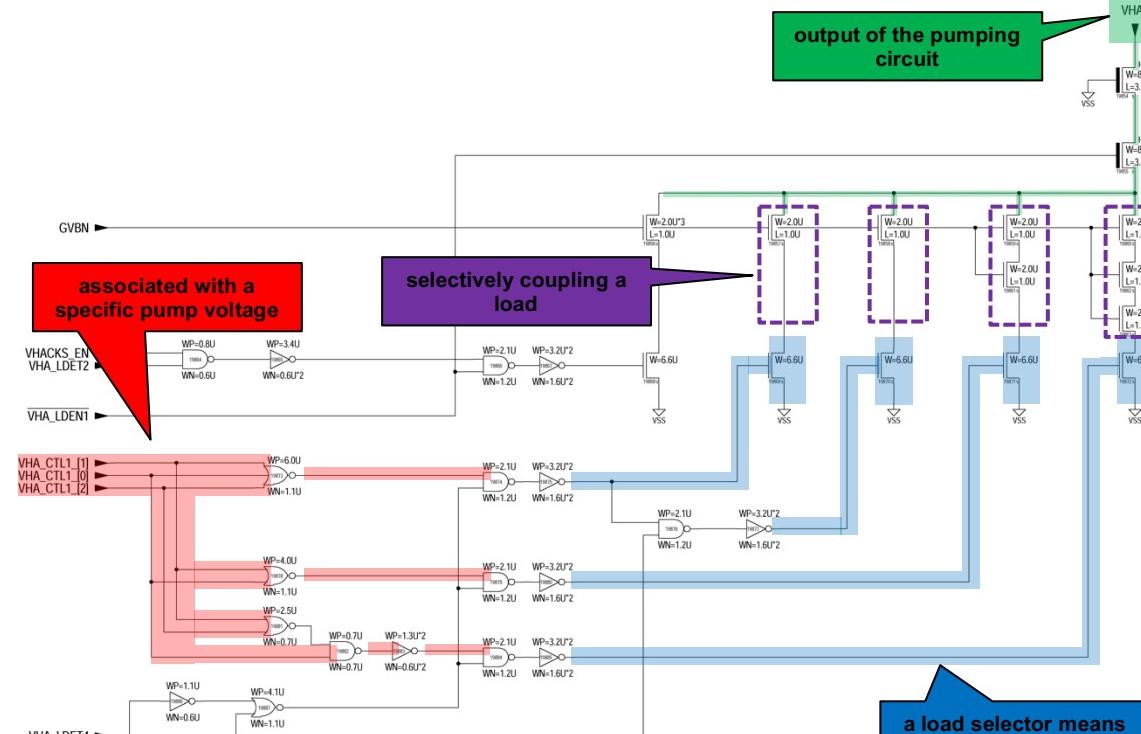
Claim 1	Accused Product
	 <p>an output of the pumping circuit</p> <p>each load associated with a specific pump voltage</p> <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.5.17.3 PNWELL Voltage Selector</p>

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 4.2.1 Wordline Voltage Switch Block 1</p>
1[c] a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit	<p>Each Accused Product includes a load selector means for selectively coupling a load associated with a specific pump voltage to the output of said pumping circuit.</p> <p>For example, the highlighted transistors below and their respective gate control signals form a load selector means. The output signal VHA_LDET4 from Level Detector 6 forms part of the load selector means. For example, the gate control signals are generated in part by a charge pump control signal (VHA_CTL1). This 3 bit value selectively couples a load associated with a specific pump voltage.</p> <p><i>See, e.g.:</i></p>



Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 1	Accused Product
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p>

Claim 2

Claim 2	Accused Products
2. The charge pump circuit of claim 1, wherein the load selector means includes a	To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means includes a target output pump selector for shutting down

Claim 2	Accused Products
<p>target output pump selector for shutting down the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref).</p>	<p>the variable charge pump circuit when the target output pump voltage (Vcfra) is greater than or equal to a reference voltage (Vref). For example, VHA2 is provided to a level detector which suspends pump clocks when a desired level is reached. VHA2 is scaled by a fixed ratio voltage divider (Voltage Divider 2). It is then compared (using Amplifier 12) to an adjustable reference voltage (generated by Reference Voltage Regulator). A 4-bit digital code CF(75:72) adjusts the output reference voltage by shorting out resistors in a resistor divider, thereby providing programmable pump output voltage levels on VHA1 and VHA2. A comparator (Amplifier 12) compares the scaled VHA2 to the programmable reference voltage. If the scaled VHA2 exceeds the programmable reference voltage, output VHA_LDET3 transitions from 1 to 0 to stop further pumping. <i>See evidence and explanation for claim element [1a], <i>supra</i>.</i></p>

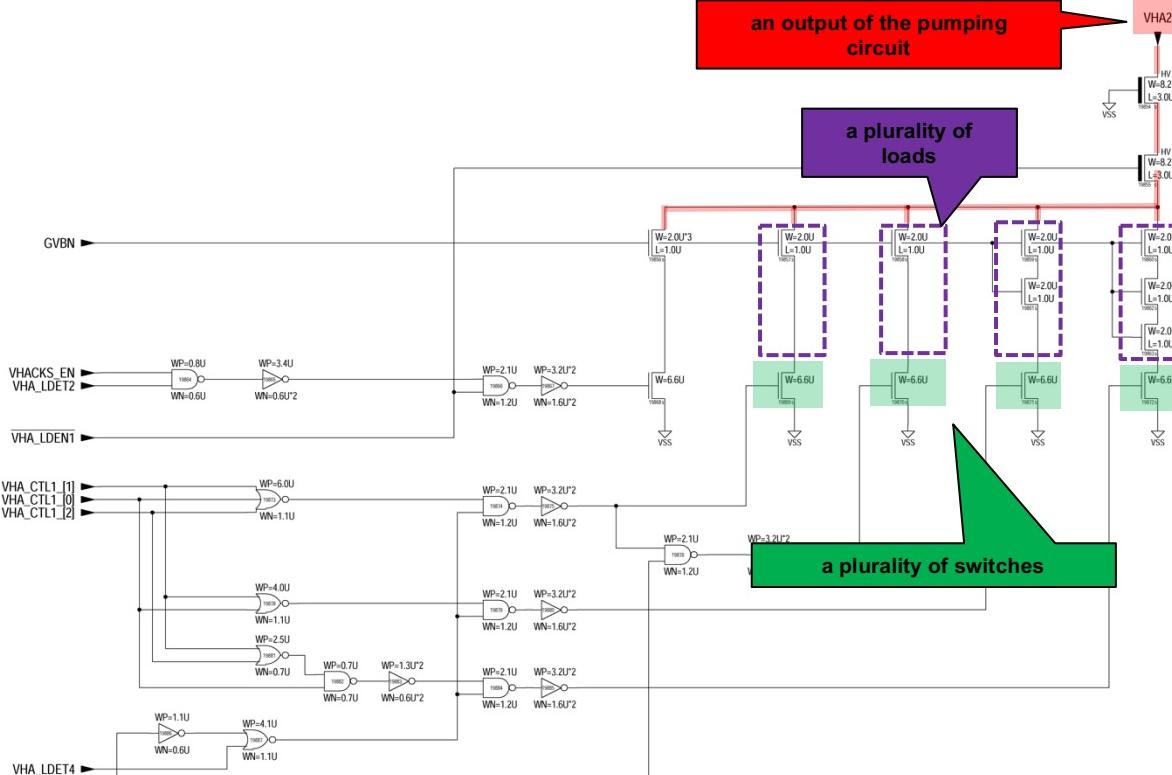
Claim 3

Claim 3	Accused Products
<p>3. The charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref).</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 2, wherein the load selector means further includes a maximum ripple on the target output selector means for adding a load, and whenever a maximum ripple on the target output voltage (Vcfrb) greater than the reference voltage (Vref) then the maximum ripple on the target output selector means adds additional loads until the Vcfrb voltage is less than or equal to the reference voltage (Vref). <i>See evidence and explanation for claim element [1a] and claim 2, <i>supra</i>.</i></p>

Claim 3	Accused Products
less than or equal to the reference voltage (Vref).	

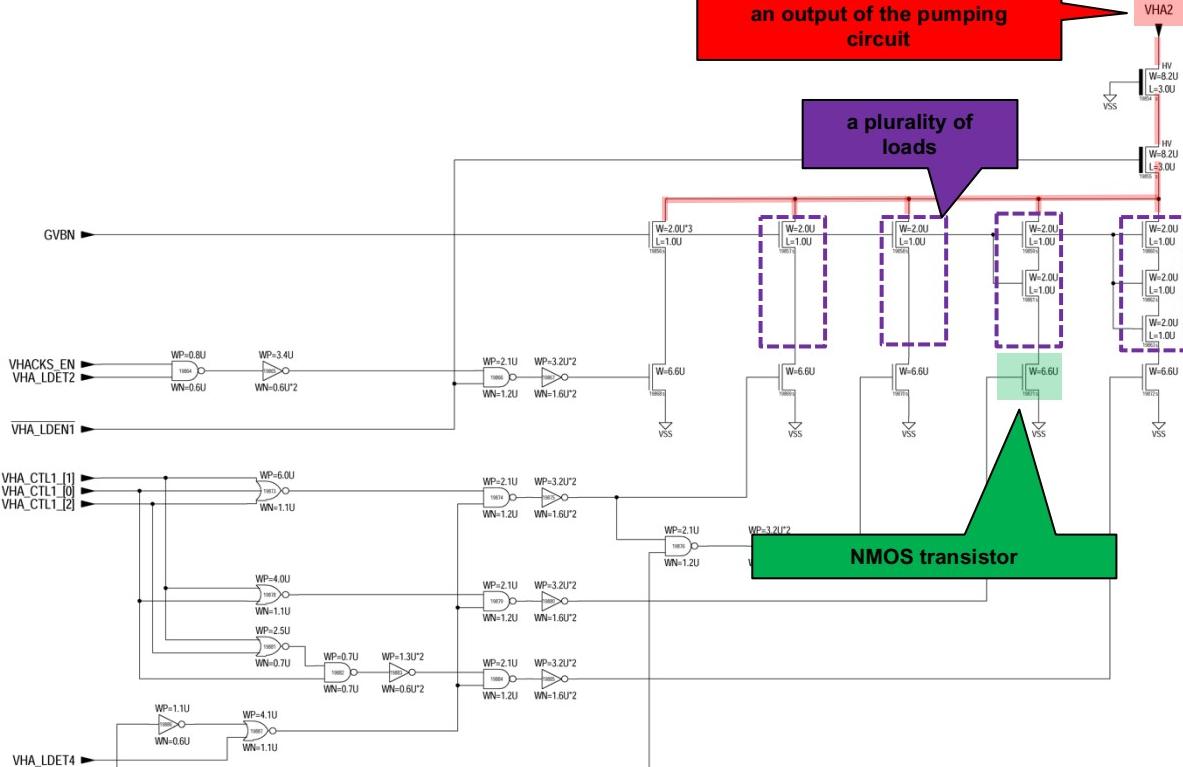
Claim 6

Claim 6	Accused Products
6. The charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein the load selector means is a plurality of switches, one switch for each of said loads, each switch having a first terminal, a second terminal, and an enable terminal, the switch being coupled in series with each load, the first terminal of the switch being coupled to the output pump and the second terminal of the switch is coupled to each load.</p> <p><i>See, e.g.:</i></p>

Claim 6	Accused Products
	 <p data-bbox="644 1101 1837 1183">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p data-bbox="644 1199 1087 1232"><i>See also claim element [1c] supra.</i></p>

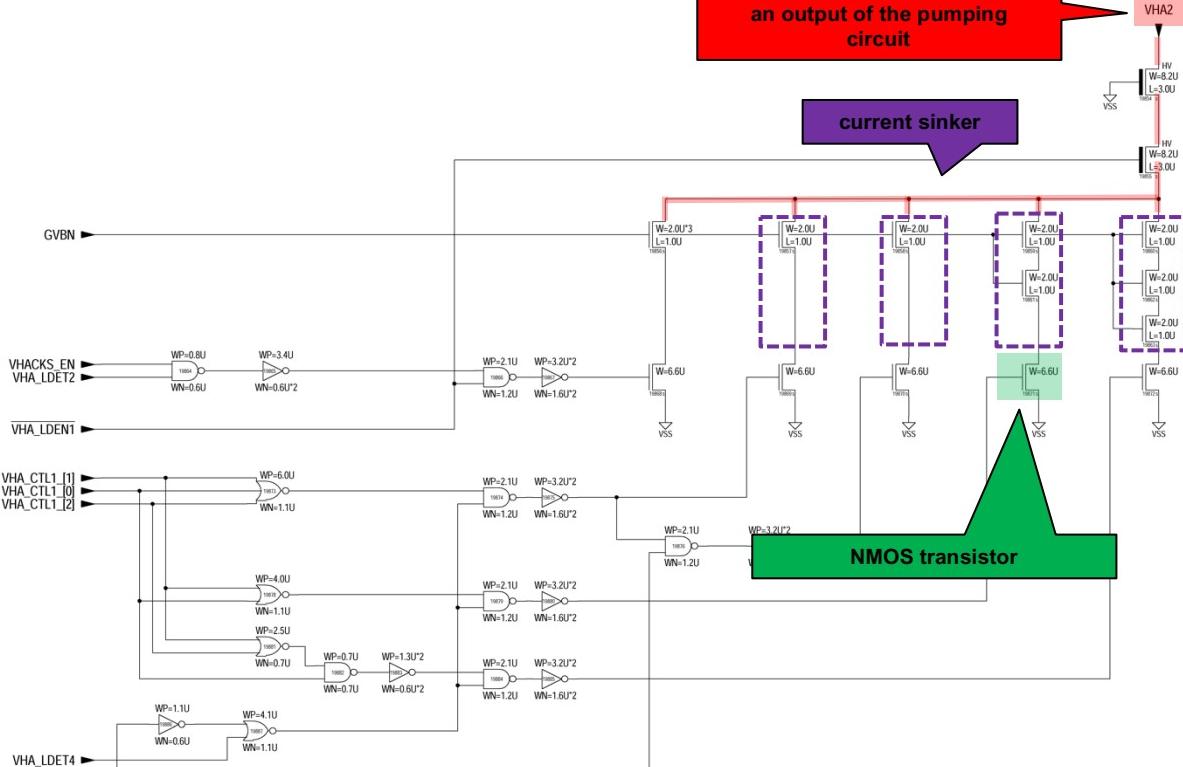
Claim 7

Claim 7	Accused Products
<p>7. The charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 1, wherein each load selector means comprises an NMOS transistor having a gate, a drain and a source, the gate of the NMOS load transistor being coupled to an enable signal, the source of the load NMOS load transistor being coupled to an electrical ground, and the drain being coupled to a load.</p> <p><i>See, e.g.:</i></p>

Claim 7	Accused Products
	 <p data-bbox="644 1109 1848 1183">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p data-bbox="644 1199 1087 1232"><i>See also claim element [1c] supra.</i></p>

Claim 8

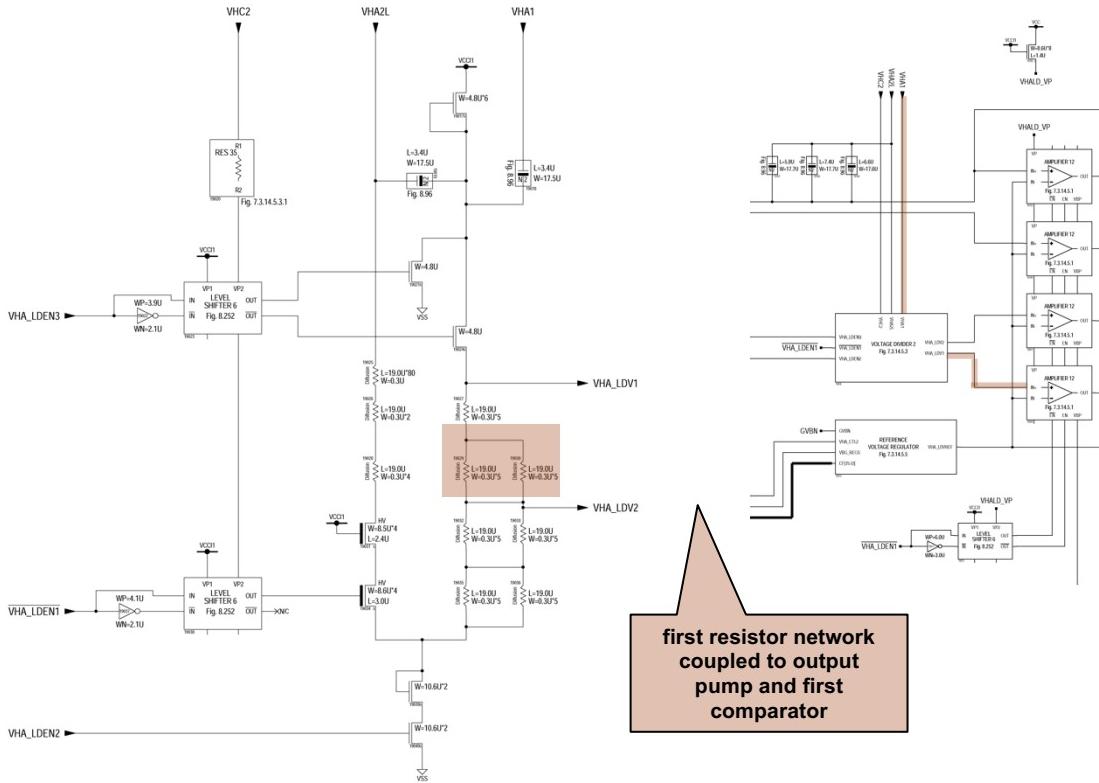
Claim 8	Accused Products
<p>8. The charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p>	<p>To the extent the preamble is limiting, each Accused Product includes the charge pump circuit of claim 7, wherein each load is a capacitor or a current sinker having a first terminal and a second terminal, the first terminal being coupled to the pump voltage and the second terminal being coupled to the drain of the NMOS transistor.</p> <p><i>See, e.g.:</i></p>

Claim 8	Accused Products
	 <p data-bbox="686 1109 1848 1183">Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.9 Current Sink 2</p> <p data-bbox="644 1199 1087 1232"><i>See also claim element [1c] supra.</i></p>

Claim 11

Claim 11	Accused Products
[11pre] 11. The charge pump circuit of claim 2 wherein the target output pump selector comprises:	<p>Each Accused Product includes the charge pump circuit of claim 2.</p> <p><i>See supra</i> claim 2.</p>
[11a] a) a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref);	<p>Each Accused Product includes a first comparator having two input terminals, an output terminal and a first enable terminal, one of the two input terminals being connected to the reference voltage (Vref).</p> <p><i>See, e.g.:</i></p>

Claim 11	Accused Products
<p>[11b] b) a first resistor network having two terminals, the first terminal being coupled to the output pump, the second terminal being coupled to one of the input terminals of the first comparator;</p>	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
	 <p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2; Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
<p>[11c] c) a second resistor network having two terminals, the first terminal being coupled to the second terminal of the first resistor network, and the second terminal of the second resistor network being</p>	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5 Level Detector 6</p>

Claim 11	Accused Products
<p>coupled to an electrical ground; and</p>	<p>Source: TechInsights CircuitVision Analysis of the Sandisk/Toshiba 05138_064G 3D NAND Flash, Figure 7.3.14.5.3 Voltage Divider 2</p>
<p>[11d] d) a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p> <p><i>See, e.g.:</i></p>	<p>Each Accused Product includes a reference voltage source (Vref) coupled to one of the input terminals of the first comparator.</p>

Claim 11	Accused Products
	<p>reference voltage source</p>